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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/026,537 | 12/27/2001 | Ihl Hyun Cho | P 282974 HD-1077/US | 9451 |

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| EXAMINER |
|---|
| RAO, SHRINIVAS H |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 11/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 10/026,537 | Applicant(s) CHO, IHL HYUN | |
|---|---|---|---|
| | Examiner Steven H. Rao | Art Unit 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *1-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *9-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

***Response to Amendment***

Applicants' amendment filed on September 05, 2002 has been entered on September 16, 2002.

Therefore claims as amended by the amendment and claims 10-19 as originally recited are currently pending I the application.

Claims 1-8 were previously withdrawn from the case.

***Election/Restrictions***

This application contains claims 1-9 drawn to an invention nonelected with traverse in Paper No. 5 A complete reply to the final rejection must include cancelation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9, 11 and 18-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Fang et al. (U.S. Patent. No. 5,858,844, herein after Fang) for reasons previously set out and reproduced below for ready reference and those set out below.

With respect to claim 9, Fang describes a method of fabricating a semiconductor device including the steps of: preparing a semiconductor substrate (Fang Fig. 1 A # 14, col. 3 line 15), forming a silicon oxide layer on the semiconductor substrate (Fang fig.! A #12, col. 3 line 43-44), forming a conductive layer on the silicon oxide layer (Fang, fig.

1A # 10, col. 3 line 44), and forming a metal oxide layer at an interface between the silicon oxide layer and the conductive layer (Fig. 1 A # 20, col. 3 lines 25-30).

With respect to claim 11, wherein the conductive layer is a metal layer or a metal nitride layer. (col. 1 lines 25-30).

With respect to claim 18, wherein the step of forming the metal oxide layer comprises of forming the metal oxide with oxygen atoms from the silicon oxide layer (Fang col. 3 lines 18-30).

With respect to claim 19, wherein the silicon oxide layer is a gate insulator and the conductive layer is a gate electrode (Fang col. 3 line 14).

For response to Applicants' arguments see Response to arguments section below.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang et al. (U.S. Patent No. 5,858,844, herein after Fang) as applied to claim 1 above, and further in view of Microchip Fabrication Text book. (herein after Van Zant).

With respect to claim 10, wherein the silicon oxide layer has a thickness of 10-100 $A^0$ Fang teaches a silicon oxide layer without specifying its thickness.

However, Microchip Fabrication, a text book by Peter Van Zant ( McGraw Hill , fourth edition) pages 511-514 in page 513 describes gate oxide thickness in the range of 100-300 $A^0$ to control the threshold voltage .

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to form a silicon oxide layer having a thickness of 10-100 $A^0$ because it was previously done in the overlapping range of 100-300 $A^0$ to form a device with the desired threshold voltage.

Wit h respect to claims 12 and 13 , wherein the metal layer comprises of at least one metal selected from a group consisting of Tungsten ( W0, tantalum ( Ta) , Titanium ( Ti) and Aluminum ( Al). ( Van Zant page 403 the motivation to combine Van Zant and fang stated above) for nitride ( see claim 11 above).

With respect to claim 14, wherein the conductive layer is 100-2000 $A^0$ ( Van Zant page 513, gate thickness 60-90 angstroms).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to form a silicon oxide layer having a thickness of 10-100 $A^0$ because it was previously done in the overlapping range of 160-90 $A^0$ to form a device with speed and other characteristics.

With respect to claim 15, wherein the step of forming the interface includes a thermal treatment at a temperature of 500-100 degrees under inert gas ambient. ( Fang claim 1 step 3 850-900 degrees).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention because includes a thermal treatment at a temperature of 500-100

degrees under inert gas ambient. it was previously done in the overlapping range of 850-900 $^{0}$ to form a device with highest saturation threshold voltage (Fang col. 4 lines 15-20).

With respect to claim 16, wherein the inert gas is selected from Nitrogen, Argon and Helium ( Van Zant page 413 use of Argon to maintain film composition).

With respect to claim 17, wherein the metal oxide layer formed has a dielectric constant of at least 3.9 .( it is an inherent property of metal oxides mentioned namely Tungsten ( W), tantalum ( Ta) , Titanium ( Ti) oxides to have a dielectric constant of 3.9 or more).

For response to Applicants' arguments see Response to arguments section below.

***Response to Arguments***

Applicant's arguments filed 9/16/2002 have been fully considered but they are not persuasive for the following reasons.

Applicants' contention with regard to the 102 rejections is that claim 9 presently recites in relevant parts , " a metal oxide layer at an interface between a silicon oxide layer and a conductive layer" and allegedly Fang teaches the gate conductive layer 10 is formed of polysilicon and therefore it would not be possible through gate oxidation process of Fang to form a metal oxide layer since no metal is present in Fang's teachings.

It is well settled law that the entire teachings of a reference as good as prior art.

It is noted that Fang col. 3 lines 42-45 states :

> A particular embodiment of the present invention is the fabrication of MOS transistors with polysilicon as the gate conductive layer 10 and silicon oxide 12 as the gate dielectric layer, and with the source and drain fabricated by the low doped drain (LDD) implant. In this particular case, the innovative gate oxidation process is a polysilicon oxidation (POX) process. The oxidation temperature and oxidation time duration for optimized transistor performances have been found to be 850° C. and 115 minutes, respectively.

and further in col.5 lines 1-5 states :

> scope thereof. The present invention can also be implemented with metal-insulator-semiconductor (MIS) field-effect transistors in general, as well as silicon-on-insulator (SOI) transistors.

Therefore Fang teaches its invention and the poly silicon gate can also be a metal gate ( when the device is a metal-insulator- semiconductor device).

Therefore Fang within its four corners teaches the use of both poly silicon ( and silicon oxide) and metal ( and metal oxide) layers.

As Fang itself teaches the interchangeable use of poly silicon and metal conductive one of ordinary skill in the art would conclude that Fang does not teach away from the instant invention.

Therefore all the presently recited limitations are taught by the applied reference Fang.

Claims 10 and 12-17 were alleged to be allowable at least for reasons presented above and by virtue of their dependence on claim 9.

However, as shown above claim 9 is not allowable and therefore claims 10 and 12 –17 are also not allowable.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

Steven H. Rao

Patent Examiner

November 5, 2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800